WHAT IS CLAIMED IS:

1. A semiconductor device in which a second conductive layer is connected through a connection pillar onto a first conductive layer embedded in a groove formed on an insulation film, wherein:

said connection pillar is formed on said first conductive layer to be self-aligned with respect to said first conductive layer without any usage of a growth guide.

2. A semiconductor device according to claim 1, wherein said first conductive layer is made of one of Al, Cu, Au and Ag.

3. A semiconductor device according to claim 1, wherein said first conductive layer is made of one of an Al alloy, a Cu alloy, an Au alloy and an Ag alloy.

4. A semiconductor device according to claim 1, wherein said connection pillar is made of one of Al, Cu, Au and Ag.

5. A semiconductor device according to claim 1, wherein said connection pillar is made of one of an Al alloy, a Cu alloy, an Au alloy and an Ag alloy.

6. A semiconductor device according to claim 1, wherein said first conductive layer and said connection pillar are made of the same metal or alloy.

7. A semiconductor device according to claim 1,

wherein said first conductive layer and said connection pillar are crystallographically aligned with each other.

8. A semiconductor device according to claim 1, wherein:

said first conductive layer and said connection pillar are made of the same metal or the alloy thereof having a face-centered cubic structure, and

said first conductive layer and said connection pillar have a <111> preferred orientation.

9. A semiconductor device according to claim 1, wherein said first conductive layer is a lower layer wiring and said second conductive layer is an upper layer wiring.

10. A semiconductor device in which a second conductive layer is connected through a connection pillar onto a first conductive layer embedded in a groove formed on an insulation film, wherein:

a growth suppression film having an opening whose width is wider than a width of said first conductive layer is formed on said insulation film and said first conductive layer, and

said connection pillar is formed on said first conductive layer within said opening of said growth suppression film to be self-aligned with respect to said first conductive layer.

11. A semiconductor device according to claim 10, wherein said first conductive layer is made of one of Al,

Cu, Au and Ag.

12. A semiconductor device according to claim 10, wherein said first conductive layer is made of one of an Al alloy, a Cu alloy, an Au alloy and an Ag alloy.

13. A semiconductor device according to claim 10, wherein said connection pillar is made of one of Al, Cu, Au and Ag.

14. A semiconductor device according to claim 10, wherein said connection pillar is made of one of an Al alloy, a Cu alloy, an Au alloy and an Ag alloy.

15. A semiconductor device according to claim 10, wherein said first conductive layer and said connection pillar are made of the same metal or alloy.

16. A semiconductor device according to claim 10, wherein said first conductive layer and said connection pillar are crystallographically aligned with each other.

17. A semiconductor device according to claim 10, wherein:

said first conductive layer and said connection pillar are made of the same metal or the alloy thereof having a face-centered cubic structure, and

said first conductive layer and said connection pillar have a <111> preferred orientation.

18. A semiconductor device according to claim 10,

wherein said growth suppression film is composed of one of a silicon oxide film, a silicon nitride film and an aluminum oxide film.

19. A semiconductor device according to claim 10, wherein said first conductive layer is a lower layer wiring and said second conductive layer is an upper layer wiring.

20. A method of manufacturing a semiconductor device, in which a second conductive layer is connected through a connection pillar onto a first conductive layer embedded in a groove formed on an insulation film, including the steps of:

forming said first conductive layer embedded in the groove formed in said insulation film; and

forming said connection pillar on said first conductive layer to be self-aligned with respect to said first conductive layer without any usage of a growth guide.

21. A method of manufacturing a semiconductor device according to claim 20, wherein said connection pillar is formed by a selective CVD method.

22. A method of manufacturing a semiconductor device according to claim 20, wherein said first conductive layer is made of one of Al, Cu, Au and Ag.

23. A method of manufacturing a semiconductor device according to claim 20, wherein said first

conductive layer is made of one of an Al alloy, a Cu alloy, an Au alloy and an Ag alloy.

24. A method of manufacturing a semiconductor device according to claim 20, wherein said connection pillar is made of one of Al, Cu, Au and Ag.

25. A method of manufacturing a semiconductor device according to claim 20, wherein said connection pillar is made of one of an Al alloy, a Cu alloy, an Au alloy and an Ag alloy.

26. A method of manufacturing a semiconductor device according to claim 20, wherein said first conductive layer and said connection pillar are made of the same metal or alloy.

27. A method of manufacturing a semiconductor device according to claim 20, wherein said first conductive layer and said connection pillar are crystallographically aligned with each other.

28. A method of manufacturing a semiconductor device according to claim 20, wherein:

said first conductive layer and said connection pillar are made of the same metal or alloy thereof having a face-centered cubic structure, and

said first conductive layer and said connection pillar have a <111> preferred orientation.

29. A method of manufacturing a semiconductor

device according to claim 20, wherein said first conductive layer is a lower layer wiring and said second conductive layer is an upper layer wiring.

30. A method of manufacturing a semiconductor device in which a second conductive layer is connected through a connection pillar onto a first conductive layer embedded in a groove formed on an insulation film, comprising the steps of:

forming said first conductive layer embedded in the groove formed on said insulation film;

forming a growth suppression film having an opening whose width is wider than a width of said first conductive layer on said insulation film and said first conductive layer, and

forming said connection pillar on said first conductive layer within said opening of said growth suppression film to be self-aligned with respect to said first conductive layer.

31. A method of manufacturing a semiconductor device according to claim 30, wherein said connection pillar is formed by a selective CVD method.

32. A method of manufacturing a semiconductor device according to claim 30, wherein said first conductive layer is made of one of Al, Cu, Au and Ag.

33. A method of manufacturing a semiconductor device according to claim 30, wherein said first conductive layer is made of one of an Al alloy, a Cu

alloy, an Au alloy and an Ag alloy.

34. A method of manufacturing a semiconductor device according to claim 30, wherein said connection pillar is made of one of Al, Cu, Au and Ag.

35. A method of manufacturing a semiconductor device according to claim 30, wherein said connection pillar is made of one of an Al alloy, a Cu alloy, an Au alloy and an Ag alloy.

36. A method of manufacturing a semiconductor device according to claim 30, wherein said first conductive layer and said connection pillar are made of the same metal or alloy.

37. A method of manufacturing a semiconductor device according to claim 30, wherein said first conductive layer and said connection pillar are crystallographically aligned with each other.

38. A method of manufacturing a semiconductor device according to claim 30, wherein:

said first conductive layer and said connection pillar are made of the same metal or alloy thereof having a face-centered cubic structure, and

said first conductive layer and said connection pillar have a <111> preferred orientation.

39. A method of manufacturing a semiconductor device according to claim 30, wherein said growth

suppression film is composed of one of a silicon oxide film, a silicon nitride film and an aluminum oxide film.

40. A method of manufacturing a semiconductor device according to claim 30, wherein said first conductive layer is a lower layer wiring and said second conductive layer is an upper layer wiring.